REMARKS

New claim 21 has been added. Claims 1, 6-8, 12, and 13 remain pending. Claims 2-5, 9-11, and 14-20 have been withdrawn without prejudice in response to a restriction requirement. Applicant asserts that the claims of the present Application are patentable over the cited art.

35 USC Section 103 Rejections

Paragraphs 6-8 of the above referenced Office Action reject independent Claims 1 and 8 as being rendered obvious by Chisholm (U.S. Patent No. 5,968,143) in view of Wood (U.S. Patent No. 6,915,363) in view of Davis (U.S. Patent No. 6,298,407) and in further view of Winkler (U.S. Pub. No. 2004/0024948). Applicants respectfully traverse.

Applicant asserts that the cited combination of references does not describe or suggest bypass registers as in the claimed embodiments. Applicant points out that the independent Claims 1 and 8 and the new claim 21 explicitly recite aspects regarding architecture of the bypass registers, for example, where Claim 1 recites a bypass register coupled to the bus master controller, wherein the bypass register is memory mapped and implements aggregation of transaction information from a host CPU by using a memory mapped data transfer. Applicants assert that these limitations are not

shown by the cited references. Similar limitations are included in independent Claim 8 and the new independent claim 21.

Each of the independent claims recites the bus master controller coupled to the disk I/O engine, a bypass register coupled to the bus master controller, an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller, and a device interface coupled to the disk I/O engine for interfacing the disk I/O. Each of the independent claims recites the bypass register is a memory mapped bypass register. Execution of a disk transaction are implemented by processing the disk transaction information from the memory mapped bypass register.

In contrast, the above referenced office action apparently relies upon Chisholm col. 5 line 5 through col. 6 line 8 to show the limitations with regard to the bypass register. Applicant has reviewed the cited section of Chisholm. The cited section of Chisholm, at col. 5 line 5, recites in part:

***

> On the local processing side 120, the command/data block transfer controller 209 includes a host DMA state machine 322 for transferring data blocks in and out of the host memory 107 over the I/O expansion bus 130. The command/data block transfer controller 209 also includes a local DMA state machine 324 for transferring data blocks in and out of the local memory 203 via the local memory controller 213.

***

Applicant finds no disclosure or suggestion regarding the command/data block transfer controller 209 using memory mapped data transfers as in the claimed invention. Applicants find no description of memory mapping, DMA transfers via memory mapped registers, or the like, or even the term memory mapped in the entire disclosure of Chisholm. This defect is not cured by the addition of Wood, Davis, and Winkler. Hence, the above referenced office action tends to piecewise combine four different references to show the functionality of the claimed invention, and still does not show a bypass register configured to use memory mapped data transfers as in each of the independent claims. Applicant requests Examiner to specifically indicate where the terminology regarding memory mapped data transfers is shown in the cited references.

Applicant also respectfully points out that the Examiner has the burden of establishing a prima facie case of obviousness. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2100-126.

With regard to the claim term "disk startup command", Claim 1 further recites the disk controller including a bus interface for interfacing with a processor and a system memory of the computer system, a disk I/O engine coupled to the bus interface, and a device interface coupled to the disk I/O engine for interfacing the disk I/O engine with a disk drive. The disk I/O engine is configured to cause a start up of the disk drive upon receiving a disk start up command from the processor, the start up command configured to hide a start latency of the disk drive. The disk I/O engine is further configured to execute a disk transaction by processing the disk transaction information from a memory mapped bypass register coupled to the disk I/O engine.

These claim limitations recite additional aspects of the architecture of the bypass registers and their functionality in control with respect to the disk I/O engine (e.g., Figure of the present application) for the Claim 1 embodiment. Applicants assert that these limitations are not shown by the cited references.

Accordingly, Claim 1 recites the disk I/O controller causing the startup of the disk drive upon receiving the command, enabling the disk controller to hide the start up latency of the disk drive, and processing this transaction information from a memory mapped bypass register. The bypass registers are memory mapped registers which functioned much faster than the prior art I/O mapped registers. Claim 8 has been amended to include similar limitations.

There is no description within Chisholm of a bus master controller coupled to the disk I/O engine, a bypass register coupled to the bus master controller, an arbiter couple to the bus master controller and the disk I/O engine, to coordinate data transfers within the disk controller, and a device interface coupled to the disk I/O engine for interfacing the disk I/O. There is no description within Chisholm of any memory mapped registers or the use of such memory mapped registers to transfer a disk I/O commands. There is no description within Chisholm of the advantages of using memory mapped bypass registers (e.g., as opposed to I/O mapped registers, etc.) for transferring disk commands.

The Wood reference is relied upon to show the transferring of a start command to an array of disk drives. The Davis reference is relied upon to show a bridge component of a computer system. Applicants point out that

the addition of Wood and Davis does not cure the defect of Chisholm. Neither would nor Davis shows disk controller memory mapped bypass registers or the use of such memory mapped bypass registers to transfer a disk I/O command.

Accordingly, Applicant asserts that Chisholm, Wood and Davis combination does not render obvious the claimed invention within the meaning of 35 USC Section 103.

With respect to dependent Claim 6 and Claim 12, Claims 6 and 12 add further limitations to the disk controller, with respect to reciting a CPB pointer buffer coupled to the disk I/O engine for dynamically appending a plurality of CPB pointers to extend to a number of disk transactions scheduled for execution by the disk I/O engine. These limitations are not shown or suggested by the cited references. The CPB pointer buffers are directly connected to the I/O engine for control in a manner independent of the arbiter. Additionally, Claims 6 and 12 have been amended to explicitly recite the CPB pointer buffers directly connected to the disk I/O engine for control independent of the arbiter.

With respect to new independent claim 21, applicant points out that claimed 21 includes all of limitations of independent claim 1, and includes a

further limitation with regard to a chain memory coupled to the disk I/O engine for buffering a plurality of CPBs to extend to a number of disk transactions scheduled for execution by the disk I/O engine. Applicant points out that the inclusion of the chain memory and its functionality is separate and distinct from the operation of the bypass register. Applicant points out that these limitations are not shown by the cited references.

CONCLUSION

Applicant respectfully asserts that all remaining claims (e.g., Claims 1, 6-8, 12, and 13) are in condition for allowance and Applicant earnestly solicits such action from the Examiner. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: October 6, 2008

/Glenn Barnes/
Glenn Barnes
Registration No. 42,293

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060